IN THE CLAIMS:

Rewrite the pending claims and add new claims as follows:

1. (currently amended) A slave device for use in a master-slave system, comprising:
a clock node to receive an externally-provided clock signal;
a phase-to-master node to receive a phase-to-master phase signal; and
a phase-from-master node to receive a phase-from-master phase signal.

2. (currently amended) The slave device of claim 1 wherein said slave device includes a delay-locked loop configured to process said clock signal and said phase-to-master signal to produce a transmit clock signal.

3. (original) The slave device of claim 2 wherein said slave device includes transmit circuitry to transmit data to a data bus in response to said transmit clock signal.

4. (currently amended) The slave device of claim 1 wherein said slave device includes a delay-locked loop configured to process said externally-provided clock signal and said phase-from-master signal to produce a receive clock signal.

5. (currently amended) The slave device of claim 4 wherein said slave device includes receive circuitry configured to receive data from a data bus in response to said receive clock signal.

6. (original) The slave device of claim 1 wherein said slave device processes a single-ended phase-to-master phase signal.

7. (original) The slave device of claim 1 wherein said slave device processes a single-ended phase-from-master phase signal.

8. (currently amended) A master-slave system, comprising:
a clock signal generator configured to produce a clock signal;
a phase signal generator configured to produce a phase signal;
a clock line connected to said clock signal generator to carry said clock signal;
a phase line connected to said phase signal generator to carry said phase signal, said phase line including a phase-to-master path to carry a phase-to-master phase signal and a phase-from-master path to carry a phase-from-master phase signal;

a master device connected to said clock line and said phase line;

a data bus connected to said master device; and

a slave device connected to said data bus, said clock line and said phase line, said slave device configured to process ~~processing~~ data on said data bus in response to said clock signal and said phase signal.

9. (original) The master-slave system of claim 8 wherein said phase signal generator includes a divide-by-N circuit to produce said phase signal from said clock signal.

10. (currently amended) The master-slave system ~~device~~ of claim 8 wherein said ~~clock and~~ phase signal generator includes a pseudo-random number generator to produce said phase signal from said clock signal.

11. (currently amended) The master-slave system ~~device~~ of claim 8 wherein said slave device includes a delay-locked loop to process said clock signal and said phase-to-master signal to produce a transmit clock signal

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12. (currently amended) The master-slave system ~~device~~ of claim 11 wherein said slave device includes transmit circuitry to transmit data to said data bus in response to said transmit clock signal.

13. (currently amended) The master-slave system ~~device~~ of claim 8 wherein said slave device includes a delay-locked loop to process said clock signal and said phase-from-master signal to produce a receive clock signal.

14. (currently amended) The master-slave system ~~device~~ of claim 13 wherein said slave device includes receive circuitry to receive data from said data bus in response to said receive clock signal.

15. (currently amended) The master-slave system ~~device~~ of claim 8 wherein said phase signal has an effective frequency that is lower than the frequency of said clock signal.

16. (currently amended) The master-slave system ~~device~~ of claim 8 wherein said phase signal is non-periodic.

17. (currently amended) A method of operating a master-slave system, said method comprising ~~the steps of~~:

generating a clock signal and a phase signal, said phase signal including a phase-to-master signal and a phase-from-master signal;

at an interface of a slave device, receiving the clock signal and phase signal;

at the slave device, transmitting data to a master device in response to said clock signal and said phase-to-master signal; and

at the slave device, receiving data from said master device in response to said clock signal and said phase-from-master signal.

18. (currently amended) The method of claim 17 wherein said transmitting data comprises:

producing a transmit clock signal having a frequency and a phase determined by said clock signal and said phase-to-master signal.

19. (original) The method of claim 18 wherein said transmitting data comprises:

operating data transmit circuitry in response to said transmit clock signal.

20. (original) The method of claim 17 wherein said receiving data comprises:

producing a receive clock signal having a frequency determined by said clock signal and said phase-from-master signal.

21. (currently amended) The method of claim 20 wherein said receiving data comprises:

operating receive circuitry in response to said receive clock signal.

22. (currently amended) The method of claim 17 wherein said generating ~~step~~ includes ~~the step of~~ generating said phase signal from said clock signal.

23. (currently amended) The method of claim 22 wherein said generating ~~step~~ includes ~~the step of~~ generating said phase signal as a divided clock signal.

24. (currently amended) The method of claim 22 wherein said generating ~~step~~ includes ~~the step of~~ generating said phase signal as a pseudo-random function of said clock signal.

25. (original) The method of claim 22 wherein said phase signal has an effective frequency that is lower than the frequency of said clock signal.

26. (original) The method of claim 22 wherein said phase signal is non-periodic.

27. (new) The method of claim 17 wherein said phase signal is non-periodic.

28. (new) The method of claim 17, wherein said master device is a memory controller and said slave device is a memory device.

29. (new) The slave device of claim 1, wherein said phase-to-master signal and said phase-from-master signal each have an effective frequency that is lower than the frequency of said clock signal.

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30. (new) The slave device of claim 1, wherein said slave device is an integrated circuit device.

31. (new) The integrated circuit device of claim 1, wherein said slave device is a memory device.

32. (new) The master-slave system of claim 8, wherein said master device is a memory controller and said slave device is a memory device.